

Digital LLRF feedbacks development, implementation and test at KEK LUCX facility

Tuesday, October 24, 2023 1:20 PM (20 minutes)

High Demand for stability, accuracy, reproducibility and monitoring capability were placed on accelerators LLRF systems, because of fundamental and applied experimental requirements. Meanwhile, availability of FPGA boards became better during last two decades. Nowadays, it is possible to implement FPGA based LLRF feedback using boards with low-bandwidth ADC&DAC (down-conversion technique). There are two options to implement feedback into the LLRF system.

The first option employs external I/Q demodulator, I/Q signals digitization, phase and amplitude calculation, PI feedback, I/Q modulation and RF signal regeneration. This approach does not require an expensive, highly stable slave oscillator or slave signal generator to down-convert picked-up signals from RF cavity. The second option is almost the same, but I/Q demodulator is implemented into the FPGA logic.

Both approaches were implemented and tested at KEK LUCX facility. This report presents feedbacks' performance results.

Keyword

Primary author: POPOV, KONSTANTIN (High Energy Accelerator Research Organization (KEK))

Co-authors: Mr ARYSHEV, ALEXANDER (High Energy Accelerator Research Organization (KEK)); Mr TERUNUMA, NOBUHIRO (High Energy Accelerator Research Organization (KEK))

Presenter: POPOV, KONSTANTIN (High Energy Accelerator Research Organization (KEK))

Session Classification: Measurement and control

Track Classification: Measurement and control