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Performance of FPGA controllers in ISAC-1 accelerator chain

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The LLRF of four of TRIUMF's ISAC-1 accelerator cavities have been replaced by 2 FPGA based system. These are 2 Drift Tube Linacs and 2 bunchers, nameley DTL4, DTL5, HEBT11 and HEBT35. The operating frequencies of these cavities 11.76 MHz, 35.36 MHz for the bunchers and 106.08 MHz for the DTLS, with the RF power ranges from 1.5 kW and 13 kW for the 2 bunchers to more than 20 kW for the DTLs. These LLRF uses internal phase locked loops for frequency generation and synchronization, feedback control using Amplitude/Phase regulations. The FPGAs also have internal stepper motor controller for resonance control. Various modes of resonance control are possible, including phase comparison and minimum seeking slide-mode control. Operational performances including frequency generation, amplitude and phase noises, tuning speeds, compatibility to original remote controls, are reported.

Keyword

FPGA, LLRF, PLL

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