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Flat gateware architecture for low level RF control

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FPGA gateware is the core component for the accelerator low level control system. A flatten architecture is introduced in this paper to improve the system modularity and so improve the code maintainability. This code architecture utilizes the new capability introduced in the system verilog, such as interface and alias to realize the design goal. A series of python and tcl scripts are developed to simplify the streamline operation from giga transceiver module implementation, verilog header generation, register/memory name and address handling as well as the iostandard/package pin assignments etc. The architecture is preliminary bench tested with the LCLS-II LLRF system and the compatibility is analyzed.

Keyword

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