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Preliminary Design of Scalable Hardware Integrated Platform for LLRF Application

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In this paper, the SHIP4LLRF (Scalable Hardware Integrated Platform for LLRF) based on 6U VPX-standard was designed preliminarily, which includes 6U mother board and two HPC FPGA mezzanine cards (FMCs). The ADC and DAC FMC is based on ADS54J60 from TI and LTC2000Y-16 form ADI, respectively. The mother board is based on Xilinx's KU060, which also features 64-bit DDR4 SDRAM, QSFP and USB3.0 interfaces. Each FMC connector is assigned 58 pairs of LVDS standard IOs and 8 pairs of GTH serial lanes. Besides, the mother board is equipped with the self-developed ZYNQBee2 module based on ZYNQ7010 for slow control such as EPICS. All ADC/DAC raw data in each SHIP4LLEF is compressed lossless without triggering and transmitted to the process board. A scalar quantization method which is in development is used for lossless compression of ADC raw data, the process board will decompress the ADC data and perform a digital algorithm to measure the amplitude and phase of the high frequency signal. This design is scalable for testing and upgradability, meanwhile, the trigger-less data transmission enable this system participate in both local (rack-scale) and accelerator-wide communication networks.

Keyword

VPX-standard, KU060, JESD204B, LLRF

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