

FPGA IMPLEMENTATION OF THE DIGITAL LOW LEVEL RF CONTROL SYSTEM FOR THE LANSCE LOW FREQUENCY BUNCHER CAVITY

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As part of the modernization of the Los Alamos Neutron Science Center (LANSCE), a digital low level RF (DLLRF) control system for the 16.67 MHz Low frequency buncher (LFB) is designed and is implemented on a Field Programmable Gate Array (FPGA). In this paper, the newly designed DLLRF control system of the LANSCE LFB and its performance verified on the cavity simulator are addressed. Since the LANSCE accelerator provides both H^+ and H^- beams that have different pulse types varying in timing and current size, the DLLRF control system of the LFB cavity requires to handle the beam type dependent multiple amplitude/phase set points, and corresponding controllers. Furthermore, in contrast to the deployed DLLRF control systems of 201.25 MHz Drift-Tube Linac (DTL), since the LFB RF frequency 16.67 MHz is subharmonic of 201.25 MHz reference, the DLLRF control system uses direct sampling, non-I/Q digital signal processing for the demodulation. For the modulation, FIR filter based Digital Hilbert Transformer (HT) is implemented to generate quadrature signals.

Keyword

LANSCE, Low frequency buncher, multiple set points,

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