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FW/SW framework for SRF cavity active resonance control

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Relater to the high precision active motion controller based on ML, we are going to describe the CI/CD pipeline for testing and deploying the FPGA FW and embedded SW for the Xilinx uBlaze processor that is in use at SLAC. We also introduce the different option to accelerate the SW using HLS flow to target FPGA FW blocks that replace the non performing code. Latest part is to describe the porting from of the XILINX uBlaze processor to the RISC-V architecture and design the CI/CD pipeline to obtain the same results with the open source architecture.

Keyword

firmware, software, CI/CD, risc-v, hls, machine learning, acceleration

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